Analog Power

AM90N03-04D

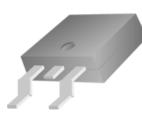
N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



FREE



PRODUCT SUMMARY

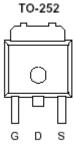
 $r_{DS(on)} m(\Omega)$

 $4.5 @ V_{GS} = 10V$

 $5.5 @ V_{GS} = 4.5V$

 $V_{DS}(V)$

30



 $I_D(A)$

87

78

Top	View
ιop	0.10044

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage		V _{DS}	30	v	
Gate-Source Voltage		V _{GS}	±20	V	
Continuous Drain Current ^a	$T_{\rm C}=25^{\circ}{\rm C}$	I _D	87	А	
Pulsed Drain Current ^b		I _{DM}	71	A	
Continuous Source Current (Diode Conduction) ^a		Is	30	Α	
Power Dissipation ^a	T _C =25°C	P _D	50	W	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Maximum	Units		
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	°C/W		
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	°C/W		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^{\circ}C$ UNLESS OTHERWISE NOTED)							
Demometer	Same al		Limits			T T •4	
Parameter	Symbol	Symbol Test Conditions		Тур	Max	Unit	
Static							
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \text{ uA}$	1		3	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = 20 V$			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 24 V, V_{GS} = 0 V$ $V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55^{\circ}C$			1 25	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 10 V$	34			А	
Drain-Source On-Resistance ^A		$V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}$			4.5	mΩ	
Drain-Source On-Resistance	r _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 6 \text{ A}$			5.5	1115.2	
Forward Tranconductance ^A	$g_{\rm fs}$	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 7 \text{ A}$		22		S	
Diode Forward Voltage	V _{SD}	$I_{S} = 7 A, V_{GS} = 0 V$		1.1		V	
Dynamic ^b							
Total Gate Charge	Q_{g}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V},$		70		nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 V, V_{GS} = 4.5 V,$ $I_{D} = 7 A$		10			
Gate-Drain Charge	Q_{gd}	ID - I H		30			
Input Capacitance	C _{iss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$		6000		pF	
Output Capacitance	C _{oss}	$\mathbf{v}_{\rm DS} = 15 \mathbf{v}, \mathbf{v}_{\rm GS} = 0 \mathbf{v},$ f = 1MHz		1000			
Reverse Transfer Capacitance	C _{rss}	I = IIVIIIZ		700			
Turn-On Delay Time	t _{d(on)}			20			
Rise Time	t _r	V_{DD} = 25 V, R_L = 25 Ω , Id = 7 A,		40		nS	
Turn-Off Delay Time	t _{d(off)}	$V_{GEN} = 10 V$		200		115	
Fall-Time	t _f			100			

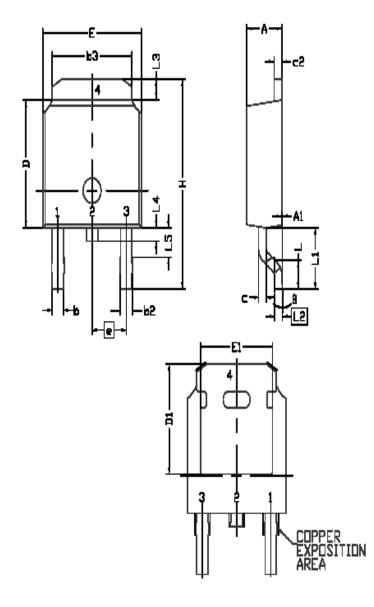
Notes

a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.

b. Guaranteed by design, not subject to production testing.

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Package Information



SYMBOL DIMENSIONAL REGMTS			
STMBUL	MIN		MAX
Ε	6.40	6.60	6.731
	140	152	1.77
1			EF
L2	C,	.508 BS	
L3	0.89	1	1,27
L4	0.64	—	1.01
L5	I	ł	
D	6.00	610	6,223
H	9,40	10,00	10,40
6	0.64	0.76	0.88
- 62	0.77	0.84	1.14
63	5,21	5.34	5,46
ſ	i	286 BS	_
A	2.20	2.30	5'36
A1	0		0.127
С	0.45	0.50	0.60
c2	0.45	0.50	0.58
M	530		
E1.	4,40	-	I
8	0"	-	10*